

AR/ 2882

Our Reference: ESI-116-B

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Patrick F. Leonard
Serial No.	09/680,342
Filing Date:	October 5, 2000
Examiner/Art Unit	C. Kao/2882
Title:	METHOD AND APPARATUS FOR EVALUATING INTEGRATED CIRCUIT PACKAGES HAVING THREE DIMENSIONAL FEATURES

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above-identified application.

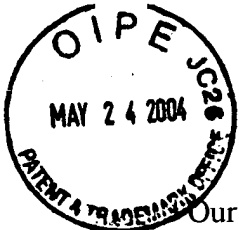
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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT
PURSUANT TO 37 C.F.R. § 1.97

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If applicable, copies of the International Search Report and any foreign patent office Search Report are enclosed for the Examiner's use, and these reports indicate the relevance of the cited references according to the respective search authorities.

These references constitute all the information of which the individuals pursuant to 37 C.F.R. § 1.56(c) are currently aware.

Respectfully submitted,

YOUNG & BASILE, P.C.

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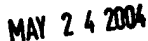
3001 West Big Beaver Rd., Suite 624
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Dated: May 21, 2004
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete if Known

Application Number	09/680,342
Filing Date	October 5, 2000
First Named Inventor	Patrick F. Leonard
Art Unit	2882
Examiner Name	C. Kao
Attorney Docket Number	ESI-116-B



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Complete if Known

Application Number	09/680,342
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Filing Date	October 5, 2000
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First Named Inventor	Patrick F. Leonard
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Art Unit	2882
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Examiner Name	C. Kao
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Attorney Docket Number	ESI-166-B
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MENGEL P: "Automated inspection of solder joints on PC board by supplementary processing of 3D and gray-level images" Signal Processing and SYStem Control.

factory Automation. Pacific Grover, Nov 27-30 1990, Proceedings of the annual conference of the Industrial Electronics Society. (IECON), New York IEEE, US Vol. 1 Conf. 16.

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